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| **logo University of Management & Technology**  School of Science & Engineering  Department of Electrical Engineering | | | |
| EL 320 Digital System Design Lab | | | |
| **Lab Schedule** | Mon 14:00 to 17:00 (Sec B)  Tues 14:00 to 17:00 (Sec C)  Wed 14:00 to 17:00 (Sec B1)  Thurs 14:00 to 17:00 (Sec C1)  Fri 11:00 to 14:00 (Sec A) | **Semester** | Fall 2013 |
| **Pre-requisite** | EE 220 Digital Logic Design  EE224 Computer Organization And  Architecture | **Hours** | 2 |
| **Instructor(s)** | Saima Shaheen (Sec A, B1)  Maryam Ali (Sec C)  Khalid Umer (Sec B)  Neaha Maham (Sec C1) | **Contact** | [Saima.shaheen@umt.edu.pk](mailto:Saima.shaheen@umt.edu.pk)  [Maryam.ali@umt.edu.pk](mailto:Maryam.ali@umt.edu.pk)  [khalid.umer@umt.edu.pk](mailto:khalid.umer@umt.edu.pk)  neaha.maham@umt.edu.pk |
| **Office** | Electrical Engineering Labs, Ground Floor | **Office Hours** | See Office Window |
| **Course Description** | This Lab explains how to go about designing complex, high-speed digital systems. A hardware description language such as Verilog will be taught to model digital systems at Behavior and RTL level. Field programmable gate arrays (FPGA) will be used in the laboratory exercises as a vehicle to understand complete design-flow. Advanced methods of logic minimization and state-machine design will be studied. Lab projects would be assigned to students. | | |
| **Expected Outcomes** | Upon completion , students will be able :   * To use computer-aided design tools for design of complex digital logic circuits * To model, simulate, verify, and synthesize with hardware description languages * To design and prototype with programmable logic | | |
| **Grading Policy** | * Lab Sessionals: 40% * Mid-term Viva/Quiz 10% * Project 30% * Final Viva 20% | | |

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| EL-327 DIGITAL SYSTEM DESIGN  **List Of Experiments** | |
| **Week** | **Experiments** |
| 1 | Implementation of ripple carry adder in verilog using XILINX ISE tools |
| 2 | Implementation of mux and decoders at behavioral level |
| 3 | Implementation of barrel shifter |
| 4 | Concept and usage of TASK and FUNCTION in verilog |
| 5 | Implementation of gate and data flow level design on FPGA |
| 6 | Implementation of combinational circuits on FPGA |
| 7 | Implementation of RAM and ROM in FPGA |
| 8 | Implementation of logic shifters , accumulators and up/down counters |
| 9 | Implementation of arithmetic logic unit on FPGA |
| 10 | Design and testing of finite state machine (FSM) |
| 11 | Design and implementation of leap year calculator on FPGA |
| 12 | Design and implementation of a real time clock on FPGA. |
| 13 | Design and testing onboard switches and LED’s in FPGA |
| 14 | Design and implementation of multiplier in FPGA |
| 15 | Design and implementation of RS-232 interface using verilog in FPGA |