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| **logoUniversity of Management & Technology**School of Science & TechnologyDepartment of Electrical Engineering |
| EL 441 Digital Electronics Lab |
| **Lab Schedule** | See Time Table | **Semester** | Spring 2013 |
| **Pre-requisite** | EE-209 Electronic Devices and Circuits | **Credit Hours** |  |
| **Instructor(s)** | 1Muhammad Salik (A,C1)2Syed Mohsin Ali (A1)3Jawadullah (C)4Jamil Ahmad (B,B1) | **Contact** | muhammad.salik@umt.ed.pksyed.mohsin@umt.ed.pkjawadullah@umt.ed.pkjamil.ahmad@umt.edu.pk |
| **Office** | Lab 6 1,2Machine Lab 3 | **Office Hours** | See office window  |
| **Teaching Assistant** | None | **Contact** | N/A |
| **Office** | N/A | **Office Hours** | N/A |
| **Lab Description** | This Lab covers simulation and designing of direct coupled, capacitor coupled inverter circuits, Schmitt trigger and different multi vibrators using transistors and 555 timer. It will elaborate the characteristics and simulation of CMOS inverter circuits and different gate implementation using CMOS. |
| **Expected Outcomes** | In accordance with HEC curriculum **outcomes** a, b, d, e, g, h & i, students at the end of the course should be able to* Get hands-on experience on Winspice
* Understand transistor switches as a building block in digital electronics
* Designing of switches and inverters
* Able to design timing and various vibrator circuits to meet given specs
* Understanding various logic gate familiesand their comparisons
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| **Grading Policy** | * Lab: 20%
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**Lab Schedule**

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| **Week** | **Experiments** |
| 1 | Simulation of Transistor Amplifier Circuit using Spice Netlists |
| 2 | Implementation and Simulation of Direct Coupled Inverter Circuit |
| 3 | Implementation and Simulation of Capacitor Coupled Inverter Circuit |
| 4 | Implementation and Simulation of Schmitt Trigger |
| 5 | Implementation and Simulation of Monostable Multivibrator |
| 6 | Implementation and Simulation of Astable Multivibrator |
| 7 | Implementation and Simulation of Bistable Multivibrator |
| 8 | Simulation of CMOS Inverter |
| 9 | Characteristics of CMOS Inverter |
| 10 | Implementation of NAND Gate using CMOS |
| 11 | Implementation of NOR Gate using CMOS |
| 12 | CMOS Inverter Layout |
| 13 | Logic Gates Layout |
| 14 | Hierarchy & Routing of 4-input AND Gate and 11-Stage Ring Oscillator |
| 15 | Decoder Circuit Layout |