University of Management & Technology
School of Science & Technology
Department of Electrical Engineering

EE224 COMPUTER ORGANIZATION AND ARCHITECTURE

Lecture Schedule	Sec A: Fri, Sat 9:30 – 11:00 Sec B: Fri, Sat 15:30-17:00 Sec C: Fri, Sat 14:00 – 15:30 Sec D: Mon, Wed 14:00-15:30 Sec E: Mon, Wed 15:30-17:00	**Semester**	Spring 2013
Pre-requisite	EE 220 – Digital Logic Design	**Credit Hours**	3 + 1
Instructor(s)	Faran Awais Butt[1] Abdullah Saqlain Sahi[2] Warda Hussain[3]	**Contact**	faran.butt@umt.edu.pk saqlain.sahi@umt.edu.pk warda.hussain@umt.edu.pk
Office	SST Campus	**Office Hours**	See office window

Course Description	This course is intended to teach the Hardware-Software interface in a microprocessor as the fundamentals of computing. The course begins with the Instruction Set Architecture (ISA) design and the use of assembly language instructions along with the various addressing modes for MIPS microprocessor. CPU performance is then evaluated both qualitatively and quantitatively. Number formats such as fixed and floating point representations are discussed in context of hardware implementations of arithmetic, logic and control instructions. The MIPS data path is thoroughly discussed in connection with single and multiple cycle approach ultimately leading to the development of pipelined processor. Pipeline data flow is studied in the light of the associated hazards along with the pipelined performance. Virtual memory system is introduced at the end along with the disk storage, buses and interfacing. These topics are in line with the HEC curriculum objectives a, d & e.
Expected Outcomes	In accordance with HEC curriculum outcomes a, b, d, e, g, h & i , students at the end of the course should be able to • Program MIPS using assembly language • Translate higher language code (C) to assembly and machine languages • Understand CPU / ALU design and evaluate its performance under a given scenario • Understand conventional single and multi-cycle data path • Appreciate pros and cons of pipelined data path • Comprehend virtual memory systems (storage disks, peripherals, etc)
Textbook(s)	**Computer Organization and Design (The Hardware / Software Interface), D.A. Patterson and J.L. Hennessy (3rd Edition)**
Grading Policy	• **Homework: 5%** (A Quiz related to homework can be taken and will be graded in homework) • **Quizzes: 15%**

	Quizzes will be 10-15 minutes. • **Midterm: 20%** 60-70 minute exam. All topics covered before the midterm exam will be included. • **Final: 40%** • 120-150 minute exam. Will be comprehensive. • **Lab: 20%** ***Note:** Passing marks for theory are 40% for theory i.e. 40/100 and 50% for lab i.e. 10/20.

Course Schedule

Lecture	Topics	Textbook (TB) / Reference (Ref) Readings
1	Basic Introduction History System Level View	**Chapter 1:** Computer Abstractions And Technology
2-9	Operations of Computer Hardware Operands of Computer Hardware Representing Instruction in Computer Logical Operations Instruction for Making Decisions Supporting Procedures in Computer Hardware MIPS Addressing	**Chapter 2:** Language of the Computer
10- 13	Signed Unsigned Number Addition Subtraction Multiplication Division	**Chapter 3:** Arithmetic for Computer
14-15	CPU Performance Factors Evaluating Performance	**Chapter 4:** Assessing and Understanding Performance
	Mid Term Exam (8th Week)	
16-21	Overview Building a Datapath Single Cycle Computer Multiple Cycle Computer Exceptions	**Chapter 5:** The Processor: Datapath and Control
22-27	Overview Pipelined Datapath Pipelined Control Data Hazards and Forwarding Data Hazards and Stalls Branch Hazards	**Chapter 6:** Enhancing Performance with Pipelining
28	Intro Basics of Cache Measuring and Improving Cache Performance Virtual Memory System	**Chapter 7:** Large and Fast: Exploiting Memory Hierarchy
29-30	Disk Storage and Dependability Networks Buses and other connections between Processor, Memory and Devices Interfacing I/O devices to the Processor, Memory and Operating Systems	**Chapter 8:** Storage, Networks and Other Peripherals
Final Term Exam (Comprehensive)		