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| **logoUniversity of Management & Technology**  School of Engineering  Department of Electrical Engineering | | | |
| EE 320 Digital System Design | | | |
| **Lecture Schedule** | Mon,Wed 15.30 to 17:00 (Sec A)  Mon,Wed 11 to 12:30 (Sec B)  Tues,Thurs 12.30 to 14:00 (SecC) | **Semester** | Fall 2013 |
| **Pre-requisite** | N/A | **Hours** | 3+1 |
| **Instructor(s)** | Imran Ali 1 (Sec B)  Muhammad Atif2 (Sec A, C) | **Contact** | Imran.ali@umt.edu.pk1  Muhammad.atif@umt.edu.pk2 |
| **Office** | Machines Lab Rooms1  S-3/412 | **Office Hours** | See Office Window |
| **Course Description** | This course explains how to go about designing complex, high-speed digital systems. A hardware description language such as Verilog will be taught to model digital systems at Behavior and RTL level. Field programmable gate arrays (FPGA) will be used in the laboratory exercises as a vehicle to understand complete design-flow. Advanced methods of logic minimization and state-machine design will be studied. The working of complex logic and memory building blocks such as memory chips, arithmetic circuits, digital processors, UARTs etc. is included. RISC and CISC architecture will also be discussed. | | |
| **Expected Outcomes** | In accordance with HEC curriculum **outcomes** a, b, d, e, g, h & i, students at the end of the course should be able to   * To use computer-aided design tools for design of complex digital logic circuits * To model, simulate, verify, and synthesize with hardware description languages * To design and prototype with programmable logic | | |
| **Textbook(s)** | **Recommended Text:**  Advanced Digital Design with the Verilog HDL by Michael D. Ciletti, Prentice Hall, 2003.  **Reference:**  Verilog HDL by Samir Palnitkar, Pearson Eduction, Second edition, 2004 | | |
| **Grading Policy** | * Assignments: 5% * Quizzes: 15% * Midterm : 20% * Final: 40% * Lab: 20% | | |

**Course Schedule**

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| **Lecture** | **Topics** | **Textbook (TB) /**  **Reference (Ref) Readings** |
| 1–2 | Introduction to digital systems and their design flow | Chapter 1 |
| 2–4 | *Verilog* introductory lecture | Chapter 4/Chapter 1,2,3 |
| 5 – 6 | Combinational Logic Design using MUX and Decoders | Chapter 2 |
| 7 – 8 | Logic Minimization techniques - McCluskey method | Chapter 2 |
| 9 – 12 | Glitches and Hazards | Chapter 2 |
| 13 – 15 | Further *Verilog* techniques | Chapter 5 |
| **Mid Term Exam (8th Week)** | | |
| 17 – 18 | Sequential Logic Design | Chapter 3 |
| 19 – 22 | Moore and Mealy State Machines Design | Chapter 3/Class Notes |
| 23 | Logic Synthesis | Chapter 6 |
| 24 | Timing Analysis and Modeling | Chapter 11 |
| 25 – 26 | Programmable Logic Devices - PAL and CPLD | Chapter 8 |
| 27 – 28 | FPGA from Xilinx and Altera | Chapter 8 |
| 29 | Advanced *Verilog* concepts - Memory, LUT and Testing | Chapter 9 |
| 30 – 31 | Architecture for Arithmetic Processors - Adders and Multipliers | Chapter 10 |
| 32 | Design for test | Chapter 11/Class Notes |
| **Final Term Exam (Comprehensive)** | | |