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| **logoUniversity of Management & Technology**  School of Science & Technology  Department of Electrical Engineering | | | |
| EE 220 Digital Logic Design | | | |
| **Lecture Schedule** | See Timetable on EED Website | **Semester** | **Fall 2013** |
| **Pre-requisite** | N/A | **Credit Hours** | 3 |
| **Instructor(s)** | Sec A: Hassan Munir  Sec B: Dr Sajjad Shami/Usman Ali  Sec D: Dr Tahir Mushtaq  Sec E: Jameel Ahmad | **Contact** | [Hassan.munir@umt.edu.pk](mailto:Hassan.munir@umt.edu.pk)  [Sajjad.shami@umt.edu.pk](mailto:Sajjad.shami@umt.edu.pk)  [Usman.ali@umt.edu.pk](mailto:Usman.ali@umt.edu.pk)  [Tahir.mushtaq@umt.edu.pk](mailto:Tahir.mushtaq@umt.edu.pk)  [Jameel.ahmad@umt.edu.pk](mailto:Jameel.ahmad@umt.edu.pk) |
| **Offices** | Top Floor, School of Engineering | **Office Hours** | See EED website |
| **Course Description** | This course covers number systems, digital waveforms, basic gates and logic functions; boolean algebra, boolean expressions; logic minimization techniques; combinational logic building blocks including decoders, encoders, multiplexers, demultiplexers, magnitude comparators; digital arithmetic, adders, subtractors; basics of sequential circuits, basic latches and flip-flops; timing parameters and diagrams; counters, shift registers; basic PLDs, CPLDs and FPGAs; architectures; binary counters and shift registers; system design with state machines; memory devices and systems including RAM, ROM and dynamic RAM. The course objectives conform to those listed in HEC guidelines as a, d & e. | | |
| **Expected Outcomes** | |  | | --- | | In accordance with HEC curriculum outcomes a, b, d, e, g, h & i, students at the  end of the course shall be able to   * Understand elements of digital logic and its application to various problems   in engineering.   * Design and analyze combinational logic circuits * Design and analyze synchronous sequential circuits | |  | | | |
| **Textbook(s)** | **Recommended Text:**   * Digital design, Edition by Morris Mano (**Required)** * Digital Design, Principles & Practices, Edition John F. Wakerly **(Recommended)** | | |
| **Grading Policy** | Final Term: 50% Mid Term: 25%  Quizzes & Assignments: 25% | | |

**Course Schedule**

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| **Lecture** | **Topics** | **Textbook (TB) /**  **Reference (Ref) Readings** |
| 1 | Introduction to digital logic | TB: Chapter 1.1 |
| 2-3 | Number Systems and Codes  Binary storage and registers  Binary logic | TB: Chapter 1.2-1.9 |
| 4 | Boolean Algebra | TB: Chapter 2.1-2.4 |
| 5-6 | Canonical and standard forms  Other logic operations | TB: Chapter 2.5-2.8 |
| 7 | The map method | TB: Chapter 3.1-3.3 |
| 8-9 | Product of Sum simplification  NAND,NOR and XOR Implementation | TB: Chapter 3.5-3.9 |
| 10-11 | Combinational logic  Analysis, Design of combinational logic  Adder/ Subtractor | TB: Chapter 4.1-4.5 |
| 12-13 | Decimal adder, Binary multiplier, Magnitude comparator | TB: Chapter 4.6-4.8 |
| 14-15 | Combinational logic Decoders, Encoders Multiplexer | TB: Chapter 4.9-4.11 |
| **Mid Term Exam (8thWeek)** | | |
| 17-18 | Synchronous Sequential logic  Latches/Flip-flops | TB: Chapter 5.1-5.4 |
| 19-22 | Analysis of clocked sequential circuits  State reduction and assignment and Design procedure | TB: Chapter 5.5, 5.7 |
| 23-24 | Shift registers | TB: Chapter 6.1-6.2 |
| 25-27 | Ripple counters, Synchronous counters and Johnson counter | TB: Chapter 6.3-6.5 |
| 28-29 | Memory and Programming logic  RAM,ROM,PLA,PAL | TB: Chapter 7 |
| 30 | Review |  |
| **Final Term Exam (Comprehensive)** | | |