**University of Management & Technology**

School of Science & Technology

Department of Electrical Engineering

|  |  |  |  |
| --- | --- | --- | --- |
| **Lecture Schedule**  | **Tue,Thu 12:30 – 13:45**  | **Semester**  | **Fall 2015** |
| **Pre-requisite**  |  **-----** | **Credit Hours**  | **3+1** |
| **Instructor(s)**  |  **Zawar Hussain**  | **Contact**  | **zawar.hussain@umt.edu.pk** |
| **Office**  | **SEN Building 5th Level Room 501** | **Office Hours**  | **See office window**  |
| **Teaching Assistant**  | **None**  | **Contact**  | **N/A**  |
| **Course Website/ Activities / Assignments**  | [**http://moodle.umt.edu.pk/**](http://moodle.umt.edu.pk/) |
| **Course Description**  | Number Systems and digital waveforms. Basic gates and logic functions. Boolean algebra, Boolean expressions. Logic minimization techniques. Combinational logic building blocks including decoders, encoders, multiplexers, demultiplexers, magnitude comparators. Digital arithmetic, adders, subtractors. Basics of circuits. Basic latches and flip-flops. Timing parameters and diagrams. Counters, shift registers. Basic PLDs, CPLDs and FPGAs architectures Binary counters and shift registers. System design with state machines. Memory devices and systems including RAM, ROM and dynamic RAM. These objectives conform to the ones listed in HEC guidelines as a, d & e. |
| **Expected Outcomes**  | In accordance with HEC curriculum outcomes a, b, d, e, g, h & i, students at the end of the course should be able to Understand * Elements of digital logic and its application to various problems in ⎫ engineering.
* Design and analyze combinational logic circuits
* Design and analyze synchronous sequential circuits ⎫
 |
| **Textbook(s)**  | **Recommended Text:** Digital Devices,$ 5^{th}$ Edition by Morris Mano**Reference:** Digital Design, Principles & Practices, $3^{rd}$ Edition by John F. WakerlyIntroduction to logic design, 3rd Edition Alan B. Marcovitz |
| **Grading Policy**  | **Final Term: 50% Mid Term: 25%** **Quizzes & Assignments: 15% Project / Presentations : 10%**  |

**Calendar of Course contents to be covered during semester**

**Course code:** EE220  **Course title:** Digital Logic Design

|  |  |  |
| --- | --- | --- |
|  **Lecture** |  **Course Contents**  | **Reference Chapter(s)** |
| 1 | Introduction to digital logic | TB: Article 1.1 |
| 2-3 | Number Systems and Codes Binary storage and registersBinary logic | TB: Articles 1.2-1.9 |
| 4 | Boolean Algebra  | TB: Articles 2.1-2.4 |
| 5-6 | Canonical and standard formsOther logic operations | TB: Articles 2.5-2.8 |
| 7 | The map method | TB: Articles 3.1-3.3 |
| 8-9 | Product of Sum simplificationNAND,NOR and XOR Implementation  | TB: Articles 3.5-3.9 |
| 10-11 | Combinational logic Analysis, Design of combinational logic Adder/ Subtractor | TB: Articles 4.1-4.5 |
| 12-13 | Decimal adder, Binary multiplier, Magnitude comparator | TB: Articles 4.6-4.8 |
| 14 | Combinational logic Decoders, Encoders Multiplexer | TB: Articles 4.9-4.11 |
| 15-16 | **Mid Term Examination** |  |

|  |  |  |
| --- | --- | --- |
| 17-18 | Synchronous Sequential logic Latches/Flip-flops  | TB: Articles 5.1-5.4 |
| 19-22 | Analysis of clocked sequential circuitsState reduction and assignment and Design procedure | TB: Articles 5.5-5.7 |
| 23-24 | Shift registers  | TB: Articles 6.1-6.2 |
| 25-27 | Ripple counters, Synchronous counters and Johnson counter | TB: Articles 6.3-6.5 |
| 28-29 | Memory and Programming logicRAM,ROM,PLA,PAL  | TB: Chapter 7 |
| 30 | Review |  |
| 31-32 | **Final Examination** |  |