**University of Management and Technology**

**Course Outline**

Course code: **EE328** Course title: **Modern Microprocessor Systems**

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| Program | BSEE |
| Credit Hours | 3 |
| Duration | One Semester |
| Prerequisites | EE 227Computer Organization and Architecture |
| Resource Person | Farah Sarwar1Jamil Ahmed2 |
| Counseling Timing | Check on Website1,2 |
| Contact | farah.sarwar@umt.edu.pk1jamil.ahmed@umt.edu.pk2 |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

The objectives of this course are to introduce students to development of microprocessor based programmable digital systems. Specifically architecture, interfacing and programming of Intel family of microprocessors are the main focus. Emphasis is put on evolution of IA-86 architecture as seen through 8008 to dual core processors. Topics related to memory & I/O interfacing, addressing modes, instruction set, microprocessor programming techniques, bus structure, DMA and interrupts are discussed. Recent research trends in modern multi-core microprocessors are also examined.

At the end of this course, students are expected to be able to:

* Identify distinguishing features of Intel family members ISA.
* Understand functions of modern memory & I/O systems and interface them to the microprocessors
* Develop software to interface microcontroller with memory and I/O.
* Analyze, design and implement practical systems of up to average complexity within a team.
* Appreciate design issues related to multi-core processor systems

**Learning Methodology:**

Lecture, Interactive, Participative

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

**Marks Evaluation Marks in percentage**

Quizzes & Assignments 15%

Mid Term 25%

Term Project 10%

Final exam 50%

Total 100

**Recommended Text Books:**

**Text books:**

1. "80X86 IBM PC and Compatible Computers: Assembly Language, Design, and Interfacing”, Volumes I & II (5th Edition) 2010, Pearson by Muhammad Ali Mazidi
2. The Intel Microprocessors (8th Edition), By Barry B. Brey

**Reference Books:**

2) Assembly Language Programming and Organization IBM PC, By Yatha Yu

**Calendar of Course contents to be covered during semester**

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|  **Week** |  **Course Contents**  | **Reference Chapter(s)** |
|  1 | **Introduction to Computing*** 1. Numbering and Coding Systems
	2. Inside the Computer
	3. Brief History of the CPU

**The 80x86 Microprocessor**1.2 Inside the 8086/8088 | Ch-01Ch-11 |
|  2 | **The 80x86 Microprocessor*** 1. Introduction to Assembly Programming
	2. Introduction to Program Segments
	3. 80x86 Addressing Modes

Introduction to PIC Controller (16F877A/ 16F887) | Ch-11 |
|  3 | **8088, 80286 Microprocessors and ISA Bus**9.1 8088 Microprocessor 9.2 8284 and 8288 Supporting Chips 9.3 8-Bit Section of ISA Bus 9.5 16-bit ISA bus | Ch-9 1 |
|  4 | **Memory Interface**10.1 Memory Devices10.2 Address Decoding | Chp-102 |
|  5 | **Memory Interfacing**10.5 32-bit Memory Interface  | Ch-102 |
|  6 | **Memory Interfacing** 10.6 64-bit Memory Interface**IO and the 8255; ISA Bus Interfacing** 11.1 8088 I/O Instructions1 | Ch-102Ch-111,2 |
|  7 | **IO and the 8255; ISA Bus Interfacing**11.2 I/O Address decoding and Design2 (pg # 387-392) 11.4 Programming and interfacing 8255 111.5 16550 Programmable Communications Interface2 (pg # 433-437) | Ch-111,2 |
|  8 | **Mid Term Examination** |  |
|  9 | **8253/54 Timer and Music**13.1 8253/54 Timer Description and Initialization13.2 IBM PC 8253/54 Timer Connections and Programming | Ch-131 |

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|  10 | **Interrupts** 12.1 Basic Interrupt Processing12.2 Hardware Interrupts | Chp 122 |
|  11 | 12.3Expanding the Interrupt Structure12.4 8259A Programmable Interrupt Controller | Chp 122 |
|  12 | **Direct Memory Access** 15.1 Concept of DMA 15.2 8237 DMA Chip Programming 15.3 8237 DMA interfacing in the IBM PC | Ch-15 |
|  13 | **Bus Interface**  15.4 The Serial COM ports 15.5 The Universal Serial Bus | Chp 152 |
|  14 | **High Speed Memory Interfacing and Cache** 22.3 Cache Memory**Pentium and RISC Processors**23.5 MMX Technology | Ch-221Ch-231 |
|  15 | **The evolution of x86: From 32-bit to 64-bit**24.1 Variations and Enhancements of 32-bit processors24.2 64-bit Architecture of x86 | Ch-241 |
| 16 | **Final Term Examination** |  |