**University of Management and Technology**

**Course Outline**

Course code: **EE445** Course title: **Digital Electronics**

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| Program | BSEE |
| Credit Hours | 3 |
| Duration | One Semester |
| Prerequisites | Electronic Devices and Circuits |
| Resource Person | Jamil Ahmed |
| Counseling Timing | Check on Website |
| Contact | [jamil.ahmed@umt.edu.pk](mailto:jamil.ahmed@umt.edu.pk) |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

Transistor inverter design and analysis. Noise margin. Fan-out. Propagation delay.

Switching speed. Detailed design of pulse and switching circuits. Monostable, Astable

and bi-stable circuits. Emitter coupled flip-flop. Schmitt trigger. Precision timing circuits,

Sweep generators. Saturating and non-saturating logic families (DTL, TTL, ECL, I2L,

CMOS). Transfer characteristics, Speed, Power consumption, Detailed study of timer ICs

and their applications, Analogue and digital circuit interface with applications,

Oscillators. Pulse Modulation and multiplexing. The course directly contributes to

**objectives** of the HEC Electrical Engineering Curriculum

**Learning Outcomes:**

In accordance with HEC curriculum students at the end of

the course should be able to

* Understand transistor switches as a building block in digital electronics
* Designing of switches and inverters
* Able to design timing and various vibrator circuits to meet given specs
* Understanding various logic gate families and their comparisons

**Teaching Methodology:**

Lectures will be used to describe and develop the concepts

Group tasks will be given to enhance interactive learning.

Industrial visits will be arranged to further strengthen the basic concepts and to increase practical exposure.

**Textbook(s)**

**Recommended Text:**

1. Solid State Pulse Circuits by David A. Bell, Reston Publishing.

2. Semiconductor Pulse and Switching Circuits by Santokh S Basi

**Reference:**

1. Digital Integrated Circuits by Jan M.Rabaey,AnanthaChandrakasan and

BorivojeNikolic

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in the semester.

**Marks Evaluation Marks in percentage**

Sessional (Quizzes + Assignments) 25%

Mid Term 25%

Final exam 50%

Total 100%

Course Schedule

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| --- | --- | --- |
| **Lecture** | **Topics** | **Textbook (TB) / Reference (Ref) Readings** |
| 1 | Introduction to Digital Electronics, Review of Ideal Semiconductor Diode; The Diode Characteristics and diode operation as a switch; Reverse recovery time and switching frequency | TB1: Ch-3, TB2: Ch- 4 |
| 2 | Bipolar Junction Transistor as a switch, Analytic expressions for BJT, BJT in saturation and cutoff. BJT switching times& improvement | TB1: Ch-4 |
| 3-4 | Calculations of switching times and frequency, design of a switch JFET and MOSFET as a switch, their characteristics, CMOS switch | TB1: Ch-4 |
| 5-6 | Design of Inverter circuits, Direct coupled and capacitor coupled inverters for various operations, JFET and Op-Amp inverters | TB1: Ch-4 |
| 7-9 | Schmitt Trigger Circuits and Voltage Comparators | TB1: Ch-6 |
| 10-13 | Monostable and AstableMultivibrators | TB1: Ch-7 |
| 14-16 | IC Timer circuits 555 timer,design and modifications to Astable and Monostable circuits | TB1: Ch-8 |
| 17 | **Midterm** |  |
| 18-19 | BistableMultivibrators, Collector and Emitter coupled circuits | TB1: Ch-13 |
| 20-21 | Bistable triggering circuits, T-Flip-Flop, SC, JK and D Flip-Flop | TB1: Ch-13 |
| 22-23 | DTL, RTL and ECL gates, I2L logic families | TB1: Ch-12 |
| 24-25 | P,N,CMOS gates, Logic gates, Fan-Out and Noise Margin | TB1: Ch-12,Ref:Ch-1 |
| 26-27 | Other TTL logic families, High Speed, Low Power and Schottky TTL | TB1: Ch-12 |
| 28-29 | Pulse Modulation Demodulation and Multiplexing Circuits | TB1: Ch-15 |
| 30 | Diode and BJT Sampling Gates, Revision of important articles | TB1: Ch-15 |
|  | **Final** |  |