**University of Management & Technology**
School of Science & Technology
Department of Electrical Engineering

# EE 219 Digital Logic Design

| | | | |
|---|---|---|---|
| **Lecture Schedule** | -Section A: Mon & Wed, 12:00-13:20<br>-Section B: Tue & Thu, 12:00-13:20<br>-Section C: Mon & Wed, 10:40-12:00<br>-Section D: Fri: 16:40-18:00, Sat: 10:40-12:00 | **Semester** | Fall 2012 |
| **Pre-requisite** | Nil | **Credit Hours** | 3 |
| **Instructor(s)** | 1- Warda Hussain, section A<br>2- Abdullah Saqlain Sahi, section B<br>3- Jawad Ullah, section C<br>**4- Dr. Waseem, section D** | **Contact** | warda.hussain@umt.edu.pk<br>saqlain.sahi@umt.edu.pk<br>jawadullah@umt.edu.pk<br>**muhammad.waseem@umt.edu.pk** |
| **Office** | C-3/14, Lab 1 cabin | **Office Hours** | See office door |
| **Teaching Assistant** | None | **Contact** | N/A |

| | |
|---|---|
| **Course Description** | The course will cover basic concepts and tools to design digital hardware consisting of both combinational and sequential logic circuits, number systems, Boolean algebra, logic gates, combinational logic design, sequential circuits and logic design, memory and simple programmable logic devices (SPLDs), introduction to field programmable logic devices (FPLDs)/field programmable gate arrays (FPGAs), introduction to HDLs (Verilog and VHDL), gate-level and dataflow modeling, use of simulation software such as Veriwell Verilog Simulator. The course directly contributes to **objectives** a, d, e and f of the HEC Electrical Engineering Curriculum. |
| **Expected Outcomes** | Upon completion of this course, students will:<br>• Have good understanding of digital logic and its application to various problems in engineering.<br>• Design and Analyze Combinational Logic circuits.<br>• Design and Analyze Synchronous Sequential Circuits.<br>• Become familiar with the FPGAs and HDLs.<br>• The course strongly supports expected **outcomes** a, b, d, g and i of the HEC Electrical Engineering Curriculum. |
| **Textbook(s)** | **Recommended Text:**<br>1- "Digital Design", by M. Morris Mano, Michael D. Ciletti , 4th Edition (PEARSON, Prentice Hall)<br>**Reference:**<br>2- "Digital Design, Principles & Practices", by John F. Wakerly, 3rd Edition. |

| | |
|---|---|
| **Grading Policy** | • Assignments & Quizzes: 20% , Midterm: 20%, Lab:20%<br>• Final Exam: 40% |

## Course Schedule

| Lecture | Topics | Textbook (TB) / Reference (Ref) Readings |
|---|---|---|
| 1 | Introduction to digital logic and design, Digital systems, Digital information, Information representation | TB: CH 1.1 |
| 2-3 | Number Systems, Arithmetic operations, Signed numbers and signed arithmetic, Decimal Codes, Alphanumeric Code; Gray Codes, Binary Logic | TB: CH 1.2-1.9 |
| 4 | Boolean Algebra | TB: CH 2.1-2.4 |
| 5-6 | Canonical and standard forms, Other logic operations (NAND, NOR, XOR) | TB: CH 2.5-2.8 |
| 7 | The Map method | TB: CH 3.1-3.3 |
| 8-9 | Product of Sum simplification,<br>NAND,NOR and XOR Implementation of Boolean functions | TB: CH 3.5-3.9 |
| 10-11 | Combinational logic circuit analysis, design of combinational logic, adder/subtractor | TB: CH 4.1-4.5 |
| 12-13 | Decimal adder, Binary multiplier, Magnitude comparator | TB: CH 4.6-4.8 |
| 14-15 | Combinational logic Decoders, Encoders, Multiplexer | TB: CH 4.9-4.11 |
| | **Mid Term Exam** | |
| 17-18 | Synchronous sequential logic<br>Latches/Flip-flops | TB: CH 5.1-5.4 |
| 19-22 | Analysis of clocked sequential circuits<br>State reduction and assignment and Design procedure | TB: CH 5.5 & 5.7 |
| 23-24 | Shift Registers | TB: CH 6.1-6.2 |
| 25-27 | Binary counters: Ripple counters, Synchronous counters and Johnson counter | TB: CH 6.3-6.5 |
| 28-29 | Memory and Programming logic<br>RAM, ROM, PLA, PAL | TB: CH 7 |
| 30 | Reserved | |
| | **Final Term Exam** | |