University of Management & Technology
School of Science & Technology
Department of Electrical Engineering

EE 327 Digital System Design

Lecture Schedule	- Sec A: Mon & Wed, 17:20-18:40 - Sec B: Tue & Thu, 13:20-14:40 - Sec C: Tue & Thu, 08:00-09:20 - Sec D: Mon & Wed, 08:00-09:20 - Sec E: Mon & Wed, 08:00-09:20	**Semester**	Fall 2012
Pre-requisite	EE 219 Digital Logic Design EE224 Computer Organization And Architecture	**Hours**	3
Instructor(s)	**Dr. Waseem** **Sec A** Ahmad Malik Sec C, E M. Asim Butt Sec B, D	**Contact**	muhammad.waseem@umt.edu.pk ahmed.malik@umt.edu.pk asim.butt@umt.edu.pk
Office	C-3/14, Lab 5, SST faculty south wing Room 3	**Office Hours**	See Office Window
Course Description	This course explains how to go about designing complex, high-speed digital systems. A hardware description language such as Verilog will be taught to model digital systems at Behavior and RTL level. Field programmable gate arrays (FPGA) will be used in the laboratory exercises as a vehicle to understand complete design-flow. Advanced methods of logic minimization and state-machine design will be studied. The working of complex logic and memory building blocks such as memory chips, arithmetic circuits, digital processors etc. is included. Memory technologies will also be discussed. A seminar is also included to introduce the students about latest trends in design technologies. The course contributes to **objectives** a, d, e and f of the HEC Electrical Engineering Curriculum.		
Expected Outcomes	In accordance with HEC curriculum **outcomes** a, b, d, e, g, h & i, students at the end of the course should be able to • To use computer-aided design tools for design of complex digital logic circuits • To model, simulate, verify, and synthesize with hardware description languages • To design and prototype with programmable logic		
Textbook(s)	**Recommended Text:** Advanced Digital Design with the Verilog HDL by Michael D. Ciletti, Prentice Hall, 2003. **Reference:** "Digital Design", by M. Morris Mano, Michael D. Ciletti , 4th Edition (PEARSON, Prentice Hall) "Verilog HDL" by Samir Palnitkar, Pearson Education, Second edition, 2004		
Grading Policy	• Assignments: 5%		

	• Quizzes: 15% • Midterm : 20% • Final: 40% • Lab: 20%

Course Schedule

Lecture	Topics	Textbook (TB) / Reference (Ref) Readings
1	**Introduction to digital systems and their design flow:** General introduction of digital world, importance, VLSI, Moore's law, design steps, verification, synthesis, physical design, layout, testing, fabrication technologies	Ciletti - Chapter 1
2-3	**Verilog introductory lectures:** ■ Language fundamental concepts, Verilog syntax and execution semantics, modules, data types, operators, statements, functions, tasks: Illustration by examples. ■ Verilog modeling, Gate level, RTL, behavioral, test bench design basics, simulation and synthesis semantics, VHDL basics, Verilog & VHDL comparison, Illustration by examples	Samir Palnitkar, Online Verilog Quick Reference Guide
4-5	**Review of Combinational Logic Design and Modeling in Verilog** ■ Arithmetic circuits: adder, subtractor (Verilog modeling) ■ Encoders, Decoders, Multiplexer, demultiplexer (Verilog modeling)	Ciletti - Chapter 2, Mano – Chapter 2
6	**Logic Minimization techniques** – K-Map method review, McCluskey method, examples	Class Notes
7-8	**Glitches and Hazards** ■ Glitches and hazards introduction, Static hazards, Mitigation of static hazards in 2 level circuits, ■ Mitigation of static hazards in multi level circuits, Dynamic hazards, Mitigation of dynamic hazards	Ciletti - Chapter 2.5
9 – 10	**Review of Sequential Logic Design** ■ Latches and Flip-Flops, Registers, Counters (Verilog modeling of sequential logic) ■ Timing diagrams, Sequential circuit analysis, Examples of Sequential circuits using Verilog	- Ciletti - Chapter 3.1, 3.2 - M. Mano - Chapter 5, 6 - Class Notes

11– 13	**Moore and Mealy State Machines Design** - Introduction to finite state machines, graphical representation, state tables, state charts - Implementation, state encoding techniques, Real life examples and FSM modeling - Verilog modeling of state machines and applications	- Ciletti - Chapter 3.4, 3,5, 3.6, 3.7 - Class Notes
14-15	**Row matching and Implication charts** - Row matching technique for state minimization in FSM - Implication charts methods for state minimization in FSM	- Ciletti - Chapter 3.8, - Class Notes
Mid Term Exam (8th Week)		
16	**Asynchronous Sequential Logic:** Analysis of asynchronous circuits , Circuits with latches, Design procedure of asynchronous circuits	M. Mano – Chapter 9.1-9.4
17-21	**Architecture for Arithmetic Processors** - Functional units for addition and subtraction: Ripple carry adder, Carry look ahead adder - Functional units for multiplication: Combinational multiplier, Sequential multiplier, Booth's algorithm - Basics of Signed binary multiplication, Basics of multiplication of fractions, Basic design of ALU of the CPU.	Ciletti - Chapter 10.1, 10.2, 10.3.1, 10.3.2, 10.3.3, 10.3.6, 10.3.7, 10.3.8, 10.3.9, 10.3.11. 10.4, 10.5
22	**Timing Analysis:** Race conditions, clock skew, slew rate , setup and hold, propagation delays, recovery time	Ciletti - Chapter 11.1, 11.2, 11.3, 11.6
23-24	**Memory technologies:** ROM, DRAM, SRAM, Flash memory	Ciletti - Chapter 8.1, 8.2
25	**Programmable Logic Devices:** - PAL, PLA and CPLD	Ciletti - Chapter 8.1, 8.3, 8.4, 8.5, 8.6 M. Mano – Chapter 7
26-27	**Field Programmable Gate Array (FPGA):** FPGA technologies, architecture, role in the ASIC market	Ciletti – Chapter 8.9, 8.10, 8.11, 8.12, 8.14, 8.15, 8.16 8.17
28	**Seminar:** State-of-the-art digital design technologies - Four topics (Electronic Design Automation, System-on-Chip (SoC), Network-on-Chip (NoC), Embedded systems)	Four presentations (15 min each) to be delivered by 4 groups of students
29-30	**Reserved for review**	
Final Term Exam (Comprehensive)		