University of Management & Technology
School of Science & Technology
Department of Electrical Engineering

EL-219 DIGITAL LOGIC DESIGN LAB

Lab Schedule	Mon 08:00-10:40 (Sec A) Wed 08:00-10:40 (Sec A1) Tues 08:00-10:40 (Sec B) Thurs 08:40-10:40 (Sec B1) Mon 14:40-17:20 (Sec C) Wed 14:40-17:20 (Sec C1) Tues 14:40-17:20 (Sec D) Thurs 14:40-17:20 (Sec D1)	**Semester**	Fall 2012
Pre-requisite	None	**Credit Hours**	1
Instructor(s)	Muhammad Hassan Qayyum Khan[1] (Sec B1 & C) Faran Awais Butt (Sec B)[2] Madiha Jalil (Sec D&D1)[3] Warda Hussain (Sec A)[4] Abdul Manan (Sec A1 and C1)[5]	**Contact**	hassan.khan@umt.edu.pk[1] faran.butt@umt.edu.pk[2] madiha.jalil@umt.edu.pk[3] warda.hussain@umt.edu.pk[4] abdul.mannan@umt.edu.pk[5]
Office	SST Campus	**Office Hours**	See office window
Teaching Assistant	None	**Contact**	N/A
Lab Work Objectives	Basic digital logic design course; topics covered include numbers systems, codes, Boolean algebra, combinational logic, arithmetic, MSI logic circuits, latches/flip flops, counters/registers, sequential circuit design, memory devices and digital electronics. These **objectives** conform to the ones listed in HEC guidelines as a, d, e, & f.		
Expected Outcomes	In accordance with HEC curriculum **outcomes** a, b, d, e, g, h & i, students at the end of the course should be able to ✓ To practically knows and perform the DLD concepts ✓ To have thorough understanding of digital logic design principles ✓ To have basic problem solving and troubleshooting techniques		
Grading Policy	**Lab Weightage : 20 % of the final grade** • **Lab Performance: 8 Marks** Each lab to be graded out of 10 in which 3 marks of attendance and 7 for performance • **Lab Test : 2 marks** To be taken on 9th week of semester i.e. after mid terms Consists of a task to be performed on the trainer board with		

	accompanied viva. • **Final** **(viva and performance): 10 marks** **(6 from project and 4 from Labs)** • **Lab Project** Any project consisting of combinational and sequential circuits to be approved by instructor of the respective sections

Lab Schedule

week	Experiment Name
1	Verification of basic binary operators and basic theorems using gates
2	Universality of NAND and NOR gates
3	Implementation of Full Adder and 4-bit Parallel Adder using IC 7483
4	Implementation of Full Subtractor and 4-bit Parallel Subtractor using IC 7483
5	Design of combinational circuits
6	Implementation of code converters using gates
7	Implementation of Encoder and Decoder using IC 74138 & 74148
8	Implementation of Multiplexer and Demultiplexer IC74151&74138
9	Verification of LATCH and FLIP FLOP operation using gates and flip flop's IC
10	Design of Sequential Circuits
11	Implementation of series and parallel registers
12	Implementation of asynchronous and synchronous counters
13	Implementation of RAM and ROM using gates and Static RAM IC
14	Implementation of LAMP HAND BALL game