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| **logo University of Management & Technology** School of Science & Technology Department of Electrical Engineering |
| EL 327 Digital System Design Lab |
| **Lab Schedule** | Mon 10:40 to 13:20 (Sec A)Wed 10:40 to 13:20 (Sec A1)Tue 10:40 to 13:20 (Sec B)Thurs 10:40 to 13:20 (Sec B1)Fri 10:40 to 13:20 (Sec C)Sat 10:40 to 13:20 (Sec C1)Fri 14:40 to 17:20 (Sec D)Sat 14:40 to 17:20 (Sec D1)Fri 08:00 to 10:40 (Sec E)Sat 08:00 to 10:40 (Sec E1) | **Semester** | Fall 2012 |
| **Pre-requisite** | EE 219 Digital Logic DesignEE224 Computer Organization And  Architecture |  **Hours** | 2 |
| **Instructor(s)** | Saima Shaheen (Sec A, A1,D,E)Ayesha Afzal (Sec B, E1)Ahmed Malik (Sec B1)Sidra Haneef (Sec C)Maryam Ali (Sec D1)Nauman Shahid (Sec C1) | **Contact** | Saima.shaheen@umt.edu.pkAyesha.afzal@umt.edu.pkAhmed.malik@umt.edu.pkSidra.haneef@umt.edu.pkMaryam.ali@umt.edu.pkNauman.shahid@umt.edu.pk |
| **Office** | Lab 5 SST3rd floor, EE-SST faculty area | **Office Hours** | See Office Window |
| **Course Description** | This Lab explains how to go about designing complex, high-speed digital systems. A hardware description language such as Verilog will be taught to model digital systems at Behavior and RTL level. Field programmable gate arrays (FPGA) will be used in the laboratory exercises as a vehicle to understand complete design-flow. Advanced methods of logic minimization and state-machine design will be studied. Lab projects would be assigned to students. |
| **Expected Outcomes** | Upon completion , students will be able :* To use computer-aided design tools for design of complex digital logic circuits
* To model, simulate, verify, and synthesize with hardware description languages
* To design and prototype with programmable logic
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| **Grading Policy** | * Lab: 20%
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| EL-327 DIGITAL SYSTEM DESIGN**List Of Experiments** |
| **Week** |  **Experiments** |
| 1 | Implementation of ripple carry adder in verilog using XILINX ISE tools |
| 2 | Implementation of mux and decoders at behavioral level |
| 3 | Implementation of barrel shifter |
| 4 | Concept and usage of TASK and FUNCTION in verilog |
| 5 | Implementation of gate and data flow level design on FPGA |
| 6 | Implementation of combinational circuits on FPGA |
| 7 | Implementation of RAM and ROM in FPGA |
| 8 | Implementation of logic shifters , accumulators and up/down counters |
| 9 | Implementation of arithmetic logic unit on FPGA |
| 10 | Design and testing of finite state machine (FSM) |
| 11 | Design and implementation of leap year calculator on FPGA |
| 12 | Design and implementation of a real time clock on FPGA. |
| 13 | Design and testing onboard switches and LED’s in FPGA |
| 14 | Design and implementation of multiplier in FPGA |
| 15 | Design and implementation of RS-232 interface using verilog in FPGA |