

**Department of Electrical Engineering,**

**School of Engineering,**

**University of Management and Technology**

**Course Outline**

**Course code……EE 320… Course title……Digital System Design…Semester Fall 2014**

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| Program | BSEE |
| Credit Hours | 3 |
| Duration | One semester |
| Prerequisites | EE220 Digital Logic Design  EE224 Computer Organization And Architecture |
| Resource Person (s) | Jameel Ahmad, Dr. Muhammad Adnan |
| Counseling Timing  (3S-33 Room#3 ) | Monday-Thursday  10am-12:30pm, |
| Contacts | Jameel Ahmad [Jameel.ahmad@umt.edu.pk](mailto:Jameel.ahmad@umt.edu.pk) (0333-558-3815)  Faran Awais Butt: faran.butt@umt.edu.pk |

Chairman/Director signature………………………………….

Dean’s signature……………………………

Date………………………………………….

**Learning Objectives:**

Course content includes the use of a hardware description language (HDL; in particular Verilog) for the specification, synthesis, simulation, and exploration of principles of register transfer level (RTL) designs. Programmable logic, such as field programmable gate array (FPGA) devices, has become an integral component of digital design. In this class the students learn how to write HDL models that can be automatically synthesized into integrated circuits using FPGAs. Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing test bench modules, and synthesizing designs to an FPGA by using automatic place and route CAD tools. Advanced methods of logic minimization and state-machine design will be studied. The working of complex logic and memory building blocks such as memory chips, arithmetic circuits, digital processors, UARTs etc. is included.

**Student Learning Outcomes:**

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| In accordance with HEC curriculum outcomes a, b, d, e, g, h & i, students at the end of the course should be able to   1. Understand issues in designing high-speed digital systems 2. Understand hardware architectures of basic building blocks of digital systems 3. Undertake design and optimization complex combinational and sequential logic 4. Describe a complex digital system using Verilog 5. Simulate and Debug digital systems using EDA tools 6. Implement digital systems on FPGA platforms 7. Analyze and specify timing in high-speed design |

**Learning Methodology:**

Lecture, interactive, participative, EDA tools and Computer Simulations

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester

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| --- | --- |
| Marks Evaluation | Marks in percentage |
| Quizzes | 15 |
| Assignments | 05 |
| Mid Term | 30 |
| Final exam | 50 |
| Total | 100 |

**Recommended Text Books:**

1. Advanced Digital Design with the Verilog HDL (2nd Edition), Michael D. Ciletti, Jan 31, 2010

**Reference Books:**

1. Digital Design with an Introduction to Verilog HDL”, by M. Morris Mano, Michael D. Ciletti, 5th Edition (Always Learning, PEARSON), 2013
2. FSM-based Digital Design using Verilog HDL by Peter Minns and Ian Elliott (Apr 28, 2008)
3. Fundamentals of Digital Logic with Verilog Design by Stephen Brown and Zvonko Vranesic (Feb 12, 2013)
4. Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog by Seetharaman Ramachandran (Jul 11, 2007)

**Course Schedule**

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| Lecture | Topics | Textbook (TB) /Reference (Ref) Readings |
| 1–2 | **Review of Combinational Logic Design:**  Combinational Logic, K-map simplification, The Quine–McCluskey algorithm (or the method of prime implicants), SOP and POS, Don’t care conditions, Designing with NAND and NOR gates, Adders/Subtractors /Encoders/Decoders, Multiplexers/De-multiplexers  Glitches and Hazards in combinational circuits-Static and Dynamic Hazards and their mitigation-2-level and multi-level Logic circuits | Chapter-2- MD Ciletti (TB)/Notes |
| 3–5 | **Review of Sequential Logic Design**  Sequential circuits Latches and Flip-Flops, Registers and Counters, Introduction to finite state machines, graphical representation, state tables, state charts, Implementation, state encoding techniques, Moore and Mealy state machines, Sequential Circuit Model, Timing of Sequential Circuits ,Sequential Circuit Design Procedure, Sequential Circuit Design Examples, State Minimization, Sequential Circuit Timing, Clock Parameters and Skew, Setup, Hold, and Propagation Delay Times in a Register for a Sequential Circuit, Metastability of Flip-flops, Synchronous design, Tristate Logic and Busses, Estimation of Maximum Clock Frequency for a sequential circuit,  Row matching and Implication charts  - Row matching technique for state minimization in FSM  - Implication charts methods for state minimization in FSM | Chapter-3-MD Ciletti(TB)/Notes/  Ciletti - Chapter 3.1, 3.2  - M. Mano - Chapter 5, 6  - Class Notes |
| 6 | **Digital System Design Flow  Methodology**  Design Methodology-An Introduction, Design Specification, Design Partition, Design Entry, Simulation and Functional Verification, Design Integration and Verification, Presynthesis Sign-Off, Gate-Level Synthesis and Technology Mapping, Postsynthesis Design Validation, Postsynthesis Timing Verification Test Generation and Fault Simulation, Placement and Routing, Physical and Electrical Design Rule Checks, Parasitic Extraction, Design Sign-Off, IC Technology Options | Chapter-1-MD Ciletti (TB) |
| 7 | **Introduction to Modeling and verification with Verilog HDL**  **Verilog HDL Basics, What is Verilog, Verilog History, Behavioral Modeling, Structural Modeling, RTL Synthesis,** | Chapter-4 MD Ciletti |
| 8-10 | **Behavioral Modeling  of Combinational Logic with Verilog**  **Behavioral Modeling,**  Behavioral Models of Multiplexers, Encoders, and Decoders  Boolean Equation-Based Behavioral Models of Combinational Logic, Basic gates realization in Verilog, Shift operations, Realization/Behavioral Modeling of MUXes/DeMuxes/Adders/Subtractors/Magnitide Comparators  A Brief Look at Data Types for Behavioral Modeling  Propagation Delay and Continuous Assignments  Dataflow Models of a Linear-Feedback Shift Register  Design Example: Keypad Scanner and Encoder | Chapter-5 MD Ciletti |
| 11-13 | **Behavioral Modeling  of Sequential Logic with Verilog**  Modeling Digital Machines with Repetitive Algorithms, Machines with multicycle operations, Intellectual Property Reuse and Parameterized Models  Clock Generators  Latches and Level-Sensitive Circuits in Verilog, Behavioral Models of Counters, Shift Registers, and Register Files, Arrays of Registers (Memories), Switch Debounce, Metastability, and Synchronizers for Asynchronous signals, Verilog modeling of state machines and applications, Pattern Sequence Detector, Machines with Multicycle Operations | Chapter-5 MD Ciletti |
| 14-15 | **A Comparison of Styles for Behavioral Modeling**  Continuous Assignment Models  Dataflow/RTL Models  Algorithm-Based Models  Writing a Test Bench for the Design  Simulation with Behavioral Models  Modeling a Test Bench  Test Bench for Combinational Circuits  Test Bench for Sequential Circuits  Simulation Using Modelsim  Simulation Results of Combinational Circuits  Simulation Results of Sequential Circuits | Chapter-5 MD Ciletti |
| Mid Term Exam (8th Week) | | |
| 17-18 | **Digital Design at the Register Transfer Level (RTL)**  Design of Register Transfer in the Data Path, Design of Control logic , Separation of Combinational and Sequential circuits, Algorithmic State Machine (ASM) Charts for Behavioral Modeling  ASMD Charts, Cyclic Behavioral Models of Flip-Flops and Latches  Cyclic Behavior and Edge Detection, Race free and Latch free design, Synchronous Logic, Synchronous Flip-flop, Realization of Time Delays, Elimination of Glitches Using Synchronous Circuits, Hold Time Violation in Asynchronous Circuits  RTL Coding Style | Mano Chapter-8  Chapter 5 MD Ciletti |
| 19-20 | **Design of Memories-Storage Devices**  ROM based implementation of Combinational Logic,  ROM based State machines,  On-chip Dual Address ROM Design-Verilog Model and verification  Single Address ROM Design- Verilog Model and verification  Verilog Model of SRAM Cell  On-Chip Dual RAM Design- Verilog Model and verification  External Memory Controller Design- Verilog Model and verification  PLA,PAL Devices, CPLD | Chapter-8 MD Ciletti |
| 21-22 | **Field Programmable Gate Array (FPGA):**  Programmable Logic Devices and Xilinx/Altera  FPGA Families, FPGA technologies, architectures, role in the ASIC market ,  Xilinx XC9500 CPLD  Xilinx XC4000 series FPGA  Xilinx New FPGA Families (Virtex, Spartan, Artix, Kintex and Zynq),  Verilog based Design flows for FPGAs  Altera End Market and Application Areas,  Altera MAX 7000 CPLD  Altera FLEX and APEX FPGAs  New Altera Families :Cyclone FPGAs , Arria FPGAs ,Stratix FPGAs, | Chapter-8 MD Ciletti |
| 23-24 | **6 Synthesis of Combinational and Sequential Logic**  6.1 Introduction to Synthesis  6.1.1 Logic Synthesis  6.1.2 RTL Synthesis  6.1.3 High-Level Synthesis  6.2 Synthesis of Combinational Logic  6.5 Synthesis of Sequential Logic with Flip-Flops  6.6 Synthesis of Explicit State Machines  6.9 Synthesis of Implicit State Machines, Registers, and Counters  6.15 Divide and Conquer: Partitioning a Design | Chapter-6 MD Ciletti |
| 25 | **Postsynthesis Design Tasks**  Post-Synthesis Design Validation. Post-Synthesis Timing Verification. Elimination of ASIC Timing Violations. False Paths. Dynamically Sensitized Paths. System Tasks for Timing Verification. Fault Simulation and Testing. Fault Simulation. JTAG Ports and Design for Testability and BIST. |  |
| 26-27 | **7 Design and Synthesis of Datapath Controllers**  7.1 Partitioned Sequential Machines  7.2 Design Example: Binary Counter  7.3 Design and Synthesis of a RISC Stored-Program Machine  7.3.1 RISC SPM: Processor  7.4 Design Example: UART Transmitter and Receiver | Chapter-7 MD Ciletti |
| 28-30 | **Architecture for Arithmetic Processors**  - Functional units for addition and subtraction: Ripple carry adder, Carry look ahead adder  - Functional units for multiplication: Combinational multiplier, Sequential multiplier, Booth’s algorithm  - Basics of Signed binary multiplication, Basics of multiplication of fractions, Basic design of ALU of the CPU  **OR**  **In-class Students Seminar: State-of-the-art digital design technologies**  - Programmable IP cores for System-on-Chip (SoC) and challenges,  -Network-on-Chip (NoC) and challenges,  -Design for Test (DFT) and challenges ,  -Xilinx SOC Solutions and Features,  Project Ideas: Traffic Light Controller Design, Real Time Clock Design, PCI Bus Arbiter, VGA Controller, Applications of FPGAs in various fields | Chapter-10 MD Ciletti  4 group Presentations |
| Final Term Exam (Comprehensive) | | |