**University of Management and Technology**

School of Engineering

Department of Electrical Engineering

**Course Outline**

Course code: EE-320L Course Title: Digital System Design Lab

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| Program | BSEE |
| Credit Hours | 1 |
| Duration | One semester |
| Prerequisites | EE 219 Digital Logic DesignEE224 Computer Organization and Architecture |
| Resource Person | Ammar Akhlaq |
| Counseling Timing(Room# ) | See Office doorsDigital System Lab, SEN Level 4 |
| Contact | ammar.akhlaq@umt.edu.pk |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

This Lab explains how to go about designing complex, high-speed digital systems. A hardware description language such as Verilog will be taught to model digital systems at Behavior and RTL level. Field programmable gate arrays (FPGA) will be used in the laboratory exercises as a vehicle to understand complete design-flow. Advanced methods of logic minimization and state-machine design will be studied. Lab projects would be assigned to students.

In accordance with HEC curriculum **outcomes** a, b, d and e, the upon completion, students will be able

* To use computer-aided design tools for design of complex digital logic circuits
* To model, simulate, verify, and synthesize with hardware description languages
* To design and prototype with programmable logic

**Learning Methodology:**

Students will perform lab experiments on simulation and hardware. The designed programmed will be practically implemented on microcontroller boards and then lab tasks/problems will be given which will be based on the technique learned in that experiment.

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

**Marks Evaluation Marks in percentage**

Lab Manuals & Performance: 40%

Final Viva or Quiz + Performance: 60%

Total 100%

**Recommended Text Books:**

**Text book:** Advanced Digital Design with the Verilog HDL by Michael D. Ciletti, Prentice Hall, 2003.

**Reference Books:**

1. Verilog HDL by Samir Palnitkar, Pearson Education, Second edition, 2004igital Design, Principles & Practices, $3^{rd}$ Edition John F. Wakerly

**Calendar of Course contents to be covered during semester**

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| **Week** | **Course Contents** | **Relevance to Theory Course** |
| 1. | Implementation of ripple carry adder in verilog using XILINX ISE tools | Chapter-2- MD Ciletti (TB)/Notes |
| 2 | Implementation of mux and decoders at behavioral level | Ciletti - Chapter 3.1, 3.2 - M. Mano - Chapter 5, 6  |
| 3 | Implementation of barrel shifter | Chapter-3-MD Ciletti(TB)/Notes/ |
| 4 | Concept and usage of TASK and FUNCTION in verilog | Chapter-1-MD Ciletti (TB) |
| 5 | Implementation of gate and data flow level design on FPGA | Chapter-1-MD Ciletti (TB) |
| 6 | Implementation of combinational circuits on FPGA | Ciletti - Chapter 3.1, 3.2 - M. Mano - Chapter 5, 6 |
| 7 | Design and testing onboard switches and LED’s in FPGA | Ciletti - Chapter 3.1, 3.2 - M. Mano - Chapter 5, 6 |
| 8 | Design and implementation of multiplier in FPGA | Ciletti - Chapter 3.1, 3.2 - M. Mano - Chapter 5, 6 |
| 9 | Implementation of RAM and ROM in FPGA | M. Mano - Chapter 7Chapter-8 MD Ciletti |
| 10 | Implementation of logic shifters , accumulators and up/down counters | M. Mano - Chapter 6.1 to 6.3 |
| 11 | Implementation of arithmetic logic unit on FPGA | Chapter-8 MD Ciletti |
| 12 | Design and testing of finite state machine (FSM) | Chapter-6 MD Ciletti |
| 13 | Design and implementation of leap year calculator on FPGA | Article …. |
| 14 | Design and implementation of a real time clock on FPGA. | Chapter-6,8 MD Ciletti |