**University of Management and Technology**

School of Engineering

Department of Electrical Engineering

**Course Outline**

**Course code:** EE 220 **Course title:** Digital Logic Design

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| Program | BSEE & BS(H) |
| Credit Hours | 3 |
| Duration | One semester |
| Prerequisites | N/A |
| Resource Persons | Ahmed MalikAyesha Iqbal |
| Counseling Timing(Room# ) | See office window |
| Contact | ahmed.malik@umt.edu.pkayesha.iqbal@umt.edu.pk |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

Upon Completion of this course, students will be able to:-

1. Understand elements of digital logic and its application to various problems in engineering
2. Design and analyze combinational logic circuits
3. Design and analyze synchronous sequential circuits

**Learning Methodology:**

Lecture, interactive, participative

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

**Marks Evaluation Marks in percentage**

Quizzes 15

Assignments 10

Mid Term 25

Attendance & Class Participation

Term Project

Presentations

Final exam 50

Total 100

**Recommended Text Books:**

**Text book:** Digital Design,$ 5^{th}$ Edition by Morris Mano & Michael Ciletti

**Reference Book:**

Digital Design, Principles & Practices, $3^{rd}$ Edition by John F. Wakerly

**Calendar of Course contents to be covered during semester**

**Course code:** EE 220  **Course title:** Digital Logic Design

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|  **Lecture** |  **Course Contents**  | **Reference Chapter(s)** |
| 1 | Introduction to digital logic | TB: Article 1.1 |
| 2-3 | Number Systems and Codes Binary storage and registersBinary logic | TB: Articles 1.2-1.9 |
| 4 | Boolean Algebra  | TB: Articles 2.1-2.4 |
| 5-6 | Canonical and standard formsOther logic operations | TB: Articles 2.5-2.8 |
| 7 | The map method | TB: Articles 3.1-3.3 |
| 8-9 | Product of Sum simplificationNAND,NOR and XOR Implementation  | TB: Articles 3.5-3.9 |
| 10-11 | Combinational logic Analysis, Design of combinational logic Adder/ Subtractor | TB: Articles 4.1-4.5 |
| 12-13 | Decimal adderBinary multiplierMagnitude comparator | TB: Articles 4.6-4.8 |
| 14 | Combinational logic DecodersEncodersMultiplexers | TB: Articles 4.9-4.11 |
| 15-16 | **Mid Term Examination** |  |

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| 17-18 | Synchronous Sequential logic Latches/Flip-flops  | TB: Articles 5.1-5.4 |
| 19-22 | Analysis of clocked sequential circuitsState reduction and assignment and Design procedure | TB: Articles 5.5-5.7 |
| 23-24 | Shift registers  | TB: Articles 6.1-6.2 |
| 25-27 | Ripple counters, Synchronous counters and Johnson counter | TB: Articles 6.3-6.5 |
| 28-29 | Memory and Programming logicRAM,ROM,PLA,PAL  | TB: Chapter 7 |
| 30 | Review |  |
| 31-32 | **Final Examination** |  |