**University of Management and Technology**

School of Engineering

Department of Electrical Engineering

**Course Outline**

Course code: EE-220L Course Title: Digital Logic Design lab

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| --- | --- |
| Program | BSEE |
| Credit Hours | 1 |
| Duration | One semester |
| Prerequisites | nil |
| Resource Person | Ahmed Malik1 (Section: D1 and D2)Maryam Ali2 (Section: A1, C1 and C2) |
| Counseling Timing(Room# ) | See Office doorsEE Labs |
| Contact | ahmed.malik@umt.edu.pk1maryam.ali@umt.edu.pk2  |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

The objective of this lab is to introduce students with basic digital logic design concepts and to implement them as well. The topics covered include numbers systems, codes, Boolean algebra, combinational logic, arithmetic, MSI logic circuits, latches/flip flops, counters/registers, sequential circuit design, memory devices and digital electronics. These **objectives** conform to the ones listed in HEC guidelines as a, d, e, & f.

In accordance with HEC curriculum **outcomes** a, b, d, e, g, h & i, students at the end of the course should be able to

* To practically knows and perform the DLD concepts
* To have thorough understanding of digital logic design principles
* To have basic problem solving and troubleshooting techniques

**Learning Methodology:**

Practicals, interactive, participative

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

**Marks Evaluation Marks in percentage**

Lab Manuals & Performance: 40%

Final Viva or Quiz + Performance: 60%

Total 100%

**Recommended Text Books:**

**Text book:** Digital Design,$4^{th}$ Edition by Morris Mano and Michael D. Ciletti

**Reference Book:**

Digital Design, Principles & Practices, $3^{rd}$ Edition by John F. Wakerly

**Calendar of Course contents to be covered during semester**

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| --- | --- | --- |
| **Week** | **Course Contents** | **Relevance to Theory Course** |
| 1 | Verification of basic binary operators and basic theorems using gates | TB: Article 2.2 – 2.8 |
| 2 | Universality of NAND and NOR gates | TB: Article 3.7 |
| 3 | Implementation of Full Adder and 4-bit Parallel Adder using IC 7483 | TB: Article 4.5 |
| 4 | Implementation of Full Subtractor and 4-bit Parallel Subtractor using IC 7483 | TB: Article 4.5 |
| 5 | Design of combinational circuits | TB: Article 4.2 |
| 6 | Implementation of code converters using gates  | TB: Article 4.4, 4.6 |
| 7 | Implementation of Encoder and Decoder using IC 74138 & 74148 | TB: Article 4.9 – 4.10 |
| 8 | Implementation of Multiplexer and Demultiplexer IC74151&74138 | TB: Article 4.11 |
| 9 | Verification of LATCH and FLIP FLOP operation using gates and flip flop’s IC | TB: Article 5.3 -5.4 |
| 10 | Design of Sequential Circuits | TB: Article 5.8 |
| 11 | Implementation of series and parallel registers | TB: Article 6.1 – 6.2 |
| 12 | Implementation of asynchronous and synchronous counters | TB: Article 6.3 – 6.4 |
| 13 | Implementation of RAM and ROM using gates and Static RAM IC | TB: Article 7.2 |
| 14 | Introduction to basic syntax of verilog and gate-level-modeling using xilinx ise tools | Material will be provided |