

University of Management and Technology

Course Outline

Course code : EE 227

Course title: Computer Organization and Architecture

Program	BSEE
Credit Hours	3
Duration	One semester
Prerequisites	Digital Logic Design
Resource Person	Faran Awais Butt Ahmed Malik
Counseling Timing (Room#)	See Office Window
Contact	faran.butt@umt.edu.pk ahmed.malik@umt.edu.pk

Chairman/Director signature.....

Dean's signature.....

Date.....

Learning Objective:

- Program MIPS using assembly language
- Translate higher language code (C) to assembly and machine languages
- Understand CPU / ALU design and evaluate its performance under a given scenario
- Understand conventional single and multi-cycle data path
- Appreciate pros and cons of pipelined data path
- Comprehend virtual memory systems (storage disks, peripherals, etc)

Learning Methodology:

Lecture, interactive, participative

Grade Evaluation Criteria

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

Marks Evaluation	Marks in percentage
Quizzes and Assignments	25
Mid Term	25
Final exam	50
Total	100

Recommended Text Books:

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Text book: Computer Organization and Design (The Hardware / Software Interface), D.A. Patterson and J.L. Hennessy (5th Edition), 2013.

(The fifth edition of *Computer Organization and Design*-winner of a 2014 Textbook Excellence Award)

Reference Book:

1. Computer Architecture, 4th Edition: A Quantitative Approach D.A. Patterson and J.L. Hennessy, 2007.

Calendar of Course contents to be covered during semester

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Week	Course Contents	Reference Chapter(s)
1	Basic Introduction History System Level View Introduction to MIPS Processor Technologies for Building Processors and Memory Performance	Chapter 1: Computer Abstractions And Technology
2	Introduction Operations of the Computer Hardware Operands of the Computer Hardware Signed and Unsigned Numbers	Chapter 2: Language of the Computer
3	Representing Instructions in the Computer Logical Operations Instructions for Making Decisions	Chapter 2: Language of the Computer
4	Supporting Procedures in Computer Hardware MIPS Addressing for 32-bit immediates and addresses	Chapter 2: Language of the Computer

5	Introduction Addition and Subtraction Multiplication	Chapter 3: Arithmetic for Computers
6	Division Floating Point	Chapter 3: Arithmetic for Computers
7	Introduction Logic Design Conventions	Chapter 4: The Processor
8	Mid Term Examination	
9	Building a Datapath	Chapter 4: The Processor
10	Completion of Data path and Control A Simple Implementation Scheme	Chapter 4: The Processor

11	An Overview of Pipelining Pipelined Datapath and Control	Chapter 4: The Processor
12	Data Hazards: Forwarding versus Stalling Control Hazards Exceptions	Chapter 4: The Processor
13	Introduction Memory Technologies The Basics of Caches	Chapter 5: Exploiting Memory Hierarchy
14	Measuring and Improving Cache Performance	Chapter 5: Exploiting Memory Hierarchy
15	Virtual Memory (tentative)	Chapter 5: Exploiting Memory Hierarchy