**University of Management and Technology**

School of Engineering

Department of Electrical Engineering

**Course Outline**

**Course code:** EE 445 **Course title:** Digital Electronics

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| --- | --- |
| Program | BSEE& BS(H) |
| Credit Hours | 3 |
| Duration | One semester |
| Prerequisites |

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| --- |
|  EE209- Electronic Devices & Circuits  |

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| Resource Persons | Ahmed Malik |
| Counseling Timing(Room# ) | See office window |
| Contact | ahmed.malik@umt.edu.pk |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

Upon Completion of this course, students will be able to:-

a) Understand of the operation of the MOS transistor.

b) Perform analysis of the wire, with interconnect and its accompanying parasitic.

c) Understand CMOS digital logic circuits.

d) Understand advanced MOS and Bipolar logic circuits

d) Design various Memory circuits to meet given specs

**Learning Methodology:**

Lecture, interactive, participative

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in a semester.

**Marks Evaluation Marks in percentage**

Quizzes 15

Assignments 10

Mid Term 25

Term Project

Presentations

Final exam 50

Total 100

**Recommended Text Books:**

1. Microelectronic Circuits by Sedra/Smith, 6th Edition

**Reference Books:**

1. Solid State Pulse Circuits by David A. Bell, Reston Publishing.

**Calendar of Course contents to be covered during semester**

**Course code:** EE220  **Course title:** Digital Logic Design

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| --- | --- | --- |
|  **Week** |  **Course Contents**  | **Reference Chapter(s)** |
| 1 | Introduction to digital circuits design. Review of the quality metrics of digital design.  | Lecture slides |
| 2 |  Static and dynamic behavior of diode  | Lecture slides  |
| 3 | Static and dynamic behavior of MOSFETs | TB: Articles 5.1 – 5.2  |
| 4 | Digital Logic Inverters  | TB: Articles 13.1 |
| 5 | The CMOS Inverter  | TB: Articles 13.2 |
| 6 | Design and Performance Analysis of the CMOS Inverter | TB: Articles 13.3 |
| 7 | CMOS Logic Gates Circuits | TB: Articles 13.4 |
| 8 | **Mid Term Examination** |  |

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| --- | --- | --- |
| 9 | *Advanced MOS and Bipolar Logic Circuits*Pseudo-NMOS Logic Circuits | TB: Articles 14.1 |
| 10 | *Advanced MOS and Bipolar Logic Circuits* Pass-Transistor Logic Circuits | TB: Articles 14.2 |
| 11 | *Advanced MOS and Bipolar Logic Circuits*Dynamic MOS Logic Circuits | TB: Articles 14.3 |
| 12 | *Advanced MOS and Bipolar Logic Circuits*BiCMOS Digital Circuits | TB: Articles 14.4 |
| 13 | *Memory and Advanced Digital Circuits*Latches and Flip-flopsSemiconductor Memories | TB: Chapter 15.1- 15.2 |
| 14 | *Memory and Advanced Digital Circuits*Random-Access MemorySense Amplifiers and Address Decoders | TB: Chapter 15.3-15.4 |
| 15 | *Memory and Advanced Digital Circuits*Read Only Memory(ROM) | TB: Chapter 15.5 |
| 16 | **Final Examination** |  |