University of Management and Technology

School of Commerce and Accountancy

Quaid e Azam Campus

Course Outline

Course Title: Digital Logic Design (CS301)	
Program	ADP(CS)
Credits Hours	3
Duration	15 Weeks / 30 Sessions
Prerequisites	
Resource Person	
Contact/Email	

Course Objectives:

The Goals the course is:

1. Introduce the concept of digital and binary systems
2. Be able to design and analyses combinational logic circuits.
3. Be able to design and analyses sequential logic circuits.
4. Understand the basic software tools for the design and implementation of digital circuits and systems.
5. Reinforce theory and techniques taught in the classroom through experiments and Projects in the laboratory.

Teaching-Learning Methodology:

Note: <u>Select methodologies as per nature of the course.</u>

- Lectures
- Recommended Text/Supplementary Texts
- Handouts
- Case Studies
- Skill Development Exercises
- Project Report/Term Paper
- Any other Teaching Tool……………………………………………

Recommended Text Book:

1. Logic and Computer Design Fundamentals — 2nd Edition
   By: M. Mano

Reference Books:

Digital fundamentals — 9th Edition
By: Floyd

Assessment & Evaluation:

Note: Please Specify the Weightage you want to assign to assignments and Final Project/ Project presentation/Presentation.

Quizzes	**15%**
Assignments	
Final Project	20%
Project Presentation/Presentations	
Mid Term	**25%**
End Term Exam	**40%**
Total:	**100**

SEHEDULE OF ACTIVITIES

Note: Please fill the tasks/activities column according to your course plan

Week	Contents/Topics to be Taught	Tasks/Activities
1	Introduction, Binary Numbers, Number Conversion Decimal Numbers	Course Outline Distribution
2	1's and 2's Complements Arithmetic Operations with unsigned numbers Arithmetic Operations with signed numbers	
3	Octal & Hexadecimal number Binary Coded Decimal (BCD) Conversions	Quiz 1
4	The Inverter, AND, OR gates NOR and NAND gates XOR and XNOR	Assignment 1
5	Boolean Algebra DeMorgan's Theorem Simplification using Boolean algebra	
6	Karnaugh Map SOP and POS expresions Karnaugh Map, SOP, POS minimization	Assignment 2
7	Basic Combinational logic circuits Universal property of NAND gates Universal property of NOR gates	Quiz 2
8	**MID TERM EXAMINATION**	

9	Combinational logic using NOR gates Combinational logic using NOR gates Basic Adders, Half Adders Full Adders	
10	Basic Subtractors Parallel binary Adders Multipliers	Quiz 3
11	Decoder Encoder Real time logic Implementation	
12	Multiplexer or Data selector De-Multiplexer Application of MUX and DeMUX	Quiz 4
13	Latches Gates Latches Edge-triggered Flip Flops	
14	Edge-Triggered Flip Flops D-Flip flop S-R Flip Flops J- K Flip Flops	Assignment 4
15	Asynchronous counter operation Synchronous counter operation SISO shift registers, SIPO shift registers PIPO shift registers	Presentations (if any)
16	**END TERM EXAMINATION**	