**University of Management and Technology**

**School of Engineering**

**Department of Electrical Engineering**

**Course Outline**

**Course code:** EE 458 **Course title:** VLSI Circuit Design

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| --- | --- |
| Program | BSEE |
| Credit Hours | 3 |
| Duration | One semester |
| Prerequisites | - |
| Resource Person(s) | T.B.A |
| Counseling Timing | T.B.A |
| Contact | T.B.A  |

**Chairman/Director signature………………………………….**

**Dean’s signature…………………………… Date………………………………………….**

**Learning Objective:**

This course provides the necessary background to design integrated circuits and systems for VLSI. These integrated circuits are required to provide very high performance while working under size, area and power constraints. The design of such electronic circuits is also complex owing to the high clock speeds, high logic density and problems in layout, simulation and fabrication. The course covers different design and architecture approaches for CMOS digital VLSI while also giving hands-on experience of design, verification and simulation of an integrated circuit using state of-the-art CAD tools. The course will cover some of the advanced topics such as Memories, Mixed-Signal circuits etc. The goal of this course is to be able to design and implement static and dynamic CMOS microelectronic circuits using VLSI technology.

**Learning Methodology:**

Interactive and participative.

**Grade Evaluation Criteria**

Following is the criteria for the distribution of marks to evaluate final grade in the semester.

**Marks Evaluation Marks in percentage**

Quizzes 10

Assignments 15

Mid Term 25

Final exam 50

Total 100

**Recommended Text Books:**

1. Digital Integrated Circuits, A Design Perspective, Second ed., Jan Rabaey, A. Chandrakasan, B. Nikolic, Prentice Hall (PHI), 2003.

2. CMOS VLSI Design: A Circuits and Systems Perspective by Neil H.E. Weste, David Harris, Fourth Edition, Pearson Education, 2011.

**Reference Books:**

Analysis and Design of Digital Integrated Circuits, David A. Hodges, Horace G. Jackson, Resve Saleh, Third Edition, McGraw Hill

**Calendar of Course contents to be covered during semester**

**Course code:** EE 458 **Course title:** VLSI Circuit Design

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| **Week** | **Course Contents**  | **Reference Chapter(s)** |
| 1 | Introduction – Microelectronics backgroundIntroduction to VLSI Design, tools, technologyLab – 1- Introduction to Simulation and Layout tools | Chap 1 (Weste) |
| 2 | MOS Transistors – characteristics, capacitance Lab – 2 – Design, simulation, layout of Inverter  | Chap 2 (Weste) |
| 3 | Advance properties in MOS Transistors, pass transistors.CMOS Processing Technology  | Chap 2 (Weste)Chap 3 (Weste) |
| 4 | CMOS Design rules, circuit extraction and layout.Lab – 3 – Delay of gates as a function of design parameters. | Chap 3 (Weste) |
| 5 | Circuit characterization – delay estimation.Power estimation, transistor sizing. | Chap 4 (Weste)Chap 5 (Weste) |
| 6 | Interconnect resistance and capacitance.Lab – 4 – Power dissipation in CMOS circuits. | Chap 6 (Weste) |
| 7 | Reliability and scaling issues. | Chap 7 (Weste) |
| 8 | **MID TERM EXAMINATION** |  |
| 9 | Combinational Logic CMOS families.Static CMOS Design. | Chap 9 (Weste)Chap 6 (Rabaey) |
| 10 | Dynamic CMOS Design.Other topics in Combinational VLSI Circuits Lab – 5 – Combinational Logic Implementation Lab Handouts. | Chap 6 (Rabaey) |
| 11 | Bi-CMOS and low-power logic circuits.Sequential Circuit: Design of Latches and Flip-flop. | Class NotesChap 10 (Weste) |
| 12 | Sequential Circuit: Sequencing and Dynamic circuits.Lab – 6- Issues in Dynamic logic circuits  | Chap 10 (Weste) |
| 13 | Synchronizer circuits for clock-domain conversion VLSI Circuits for SRAM and CAM.Lab – 7 – SRAM Design issues . | Chap 10 (Weste)Chap 12(Weste) |
| 14 | I/O Pads for VLSI Chips Design case studies (advanced topics)  | Chap 13 (Weste) |
| 15 | Mixed-Signal Circuit Student Projects | Class Notes |